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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,300	11/17/2006	Shigeharu Yamagami	8017-1200	7452

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EXAMINER	
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ART UNIT	PAPER NUMBER
4148	

MAIL DATE	DELIVERY MODE
04/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,300	YAMAGAMI ET AL.	
	Examiner	Art Unit	
	Andres Munoz	4148	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 2, 4, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17 and 18**, are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,756,643 B1 (hereinafter "Achuthan").

Regarding claim 1, Achuthan teaches a semiconductor device comprising a first semiconductor region (810 Fig. 8) and a second semiconductor region (801/802 Fig. 8), wherein a field effect transistor (Fig. 7) is comprised of the first semiconductor region comprising at least one semiconductor layer(s) (210 Fig. 3) protruding upward from a substrate (110 Fig. 3), a gate electrode(s) (820 Fig. 8) formed via an insulating film (140 and 310 Fig. 3) such that the gate electrode(s) strides over the semiconductor layer(s) and source/drain regions provided in the semiconductor layer(s) on both sides of the gate electrode(s),whereby a channel region is formed in at least both side surfaces of the semiconductor layer(s). (Figs. 7 & 8, Col. 3 lines: 45-53, Col. 4 lines: 45-67)

Achuthan further teaches the second semiconductor region comprises semiconductor layers protruding upward from the substrate (801 and 802 Fig. 8) and placed, at least opposing the first semiconductor region at both ends in the direction

perpendicular to a channel current direction and the side surfaces of the semiconductor layers facing the first semiconductor region are parallel to the channel current direction. (Fig. 8, Col. 5 lines 11-23).

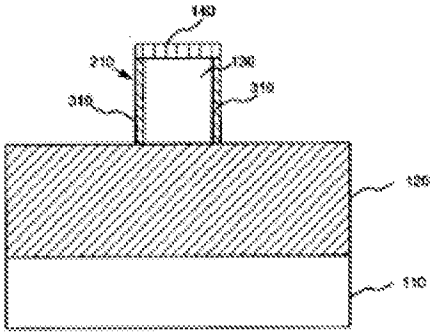

Fig. 3

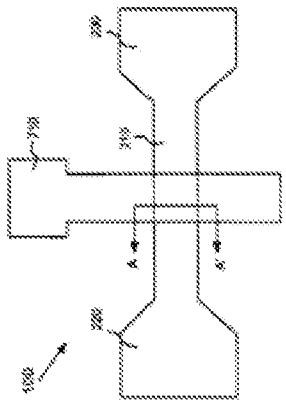

Fig. 7

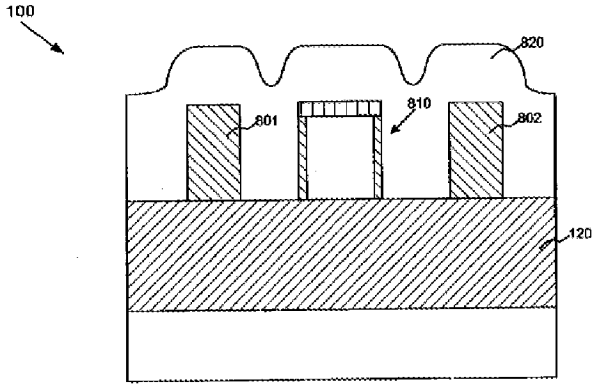

Fig. 8

Regarding claim 2, Achuthan teaches the first semiconductor region comprises a plurality of the semiconductor layers aligned such that the channel current direction is mutually parallel (Fig. 9, Col 5. lines: 24-30 – “901 may represent fins….used in the FinFETs. Lines 902 represent dummy fins").

Regarding claim 4, Achuthan teaches the gate electrode(s) is formed such that the gate electrode(s) strides over at least two of the plurality of the semiconductor layers (Figs. 7-10 - Col 5 lines: 24-30.)

Regarding claim 7, Achuthan teaches that in the direction perpendicular to the channel current direction, an additional semiconductor layer in the second semiconductor region is formed between the plurality of the semiconductor layers in the first semiconductor region (Fig. 8 and Fig. 10 – Col. 5, lines: 31-46 - "Dummy structure 1002 encompasses….provide better uniformity during planarization").

Regarding claim 8, Achuthan teaches the plurality of the semiconductor layers are aligned at even intervals in the direction perpendicular to the channel current direction (Fig. 9 &10 – Col 5, lines: 24-42).

Regarding claim 9, Achuthan teaches the semiconductor layers in the second semiconductor region formed in both sides of the first semiconductor region are disposed at even intervals from the first semiconductor region (Fig. 8-10 – Col. 5, lines: 11-46).

Regarding claim 10, Achuthan teaches the semiconductor layer(s) in the first semiconductor region and the semiconductor layers in the second semiconductor region are aligned at even intervals in the direction perpendicular to the channel current direction (Fig. 8-10 – Col. 5, lines: 11-46).

Regarding claim 11, Achuthan teaches the gate electrode(s) is formed, extending from over the semiconductor layer(s) in the first semiconductor region to over

the semiconductor layers in the second semiconductor region (Fig. 8, Col. 5 lines 11-23).

Regarding claims 13 and 14, Achuthan teaches at least a part covered by the gate electrode(s) in the semiconductor layer(s) in the first semiconductor region has a substantially cuboid shape (Figs. 2A & 7); and the semiconductor layer(s) in the first semiconductor region has a substantially cuboid shape (Fig. 9, Col 5. lines: 24-30).

Regarding claim 15, Achuthan teaches that in the channel current direction, a length of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is longer than a length of the gate electrode(s). (Fig. 9-10 – Col. 5, lines: 24-46 – "The dimension of dummy structure....depend on the overall pattern density being used in the semiconductor device.").

Regarding claim 16, Achuthan teaches that in the channel current direction, a length of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is equal to or larger than a length of the semiconductor layer(s) in the first semiconductor region. (Fig. 9-10 – Col. 5, lines: 24-46).

Regarding claim 17, Achuthan teaches that in the direction perpendicular to the channel current direction, a width of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is equal to or larger than a width of the semiconductor layer(s) in the first semiconductor region (Fig. 9-10 – Col. 5, lines: 24-46 – "The dimension of dummy structure....depend on the overall pattern density being used in the semiconductor device.").

Regarding claim 18, Achuthan teaches the second semiconductor region further comprises a pair of semiconductor layers which connects from one semiconductor layer to the other semiconductor layer of the semiconductor layers in both sides of the first semiconductor region such that the second semiconductor region surrounds the first semiconductor region (Fig. 10 – Col. 5, lines: 31-46).

3. **Claims 19, 20, 21, 22, 23, 25, 27, 29, 30, 31, 32, 33, 34, 35, 36, 37 and 38**, are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,756,643 B1 (hereinafter "Achuthan").

Regarding claim 19, Achuthan teaches a process for manufacturing a semiconductor device, comprising the steps of: forming fin-type semiconductor layers for forming a first semiconductor region (810 Fig. 8) comprising at least one semiconductor layer(s) protruding upward from a substrate and a second semiconductor region (801/802 Fig. 8) comprising semiconductor layers protruding upward from the substrate at least in both sides sandwiching the first semiconductor region (Fig. 10 – Col. 5, lines: 31-46); and forming a transistor (Fig. 7) by forming a gate electrode(s) (820 Fig. 8) striding over the semiconductor layer(s) in the first semiconductor region, an insulating film between the gate electrode(s) (140/310 Fig. 3) and at least both side surfaces of the semiconductor layer(s) and source/drain regions in both sides sandwiching the gate electrode(s) in the semiconductor layer(s). (Fig. 7) (Col. 3 lines: 45-53, Col. 4 lines: 45-67, Col. 5 lines 11-23).

4. **Regarding claim 20, 21 and 22**, Achuthan teaches the first semiconductor region and the second semiconductor region are formed such that the side surface of the second semiconductor region in the side of the first semiconductor region is parallel to a channel current direction; the first semiconductor region and the second semiconductor region are simultaneously formed by processing a semiconductor substrate on the substrate into a predetermined shape; and the processing into the predetermined shape is conducted by etching the semiconductor substrate using a mask having a shape corresponding to the first semiconductor region and the second semiconductor region. (Fig. 8 & 9, Col. 5 lines: 11-30 and Col. 3 lines: 22-39).

Regarding claim 23, Achuthan teaches the gate electrode(s) is formed such that the gate electrode(s) extends from over the semiconductor layer(s) in the first semiconductor region to over the semiconductor layers in the second semiconductor region (Fig. 8, Col. 5 lines 11-23).

Regarding claim 25, Achuthan teaches a plurality of the semiconductor layers are formed as the first semiconductor region such that direction of channel current flowing in the individual semiconductor layers is mutually parallel (Fig. 9-10 – Col. 5, lines: 24-46).

Regarding claim 27, Achuthan teaches the process wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) strides over at least two or more of the plurality of the semiconductor layers in the first semiconductor region (Figs. 7-10 - Col 5 lines: 24-30).

Regarding claim 29, Achuthan teaches that in the step of forming the fin-type semiconductor layers, an additional semiconductor layer in the second semiconductor region is formed between the semiconductor layers in the first semiconductor region (Fig. 8 and Fig. 10 – Col. 5, lines: 31-46 - "Dummy structure 1002 encompasses….provide better uniformity during planarization") .

Regarding claim 30, Achuthan teaches the plurality of the semiconductor layers in the first semiconductor region are formed at even intervals in the direction perpendicular to the channel current direction (Fig. 9 &10 – Col 5, lines: 24-42).

Regarding claim 31, Achuthan teaches the semiconductor layers in the second semiconductor region are disposed in both sides of the first semiconductor region at even intervals from the first semiconductor region (Fig. 8-10 – Col. 5, lines: 11-46).

Regarding claim 32, Achuthan teaches the plurality of the semiconductor layers in the first semiconductor region and the semiconductor layers in the second semiconductor region are formed at even intervals in the direction perpendicular to the channel current direction (Fig. 8-10 – Col. 5, lines: 11-46).

Regarding claims 33 and 34, Achuthan teaches at least a part covered by the electrode gate(s) in the semiconductor layer(s) in the first Semiconductor region are formed such that the part has a substantially cuboid shape (Figs. 2A & 7); and the semiconductor layer(s) in the first semiconductor region are formed such that the semiconductor layer(s) has a substantially cuboid shape (Fig. 9, Col 5. lines: 24-30).

Regarding claim 35, Achuthan teaches the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such

that a length of the semiconductor layers in the channel current direction is longer than a length of the gate electrode(s). (Fig. 9-10 – Col. 5, lines: 24-46).

Regarding claims 36 and 38, Achuthan teaches the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a length of the semiconductor layers in the channel current direction is longer than a length of the semiconductor layer(s) in the first semiconductor region; and a pair of semiconductor layers are further formed as the second semiconductor region, which connects from one semiconductor layer to the other semiconductor layer of the semiconductor layers in both sides of the first semiconductor region such that the second semiconductor region surrounds the first semiconductor region (Fig. 10 – Col. 5, lines: 31-46).

Regarding claim 37, Achuthan teaches that in the step of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a width of the semiconductor layers in the direction perpendicular to the channel current direction is equal to or larger than a width of the semiconductor layer(s) in the first semiconductor region (Fig. 9-10 – Col. 5, lines: 24-46 – “The dimension of dummy structure....depend on the overall pattern density being used in the semiconductor device.").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 3**, is rejected under 35 U.S.C. 103(a) as being unpatentable over US Achuthan, in view of US 6,642,090 B1 (hereinafter "Fried").

Regarding claim 3, Achuthan teaches a separate source/drain regions and a separate gate electrode formed on a semiconductor layer in the first semiconductor region, but does not explicitly teach a plurality of semiconductor layers with separate source/drain regions and separate gate electrodes.

Fried teaches separate source/drain regions (220) and separate gate electrodes (222) are formed to each of the plurality of the semiconductor layers in the first semiconductor region (Fig. 7, Col. 8 lines: 60-66, Col. 9 lines: 1-2).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device as disclosed by Achuthan by incorporating a plurality of devices as taught by Fried. The motivation would have been to use FinFETs based logic devices (Fried – Col. 9 lines: 3-39).

6. **Claims 5 and 6**, are rejected under 35 U.S.C. 103(a) as being unpatentable over US Achuthan, in view of US 6,909,147 B2 (hereinafter "Aller")

Regarding claims 5 and 6, Achuthan teaches a source/drain regions and a gate electrode formed on a semiconductor layer in the first semiconductor region, but does not explicitly teach arrangements of gate electrode(s) and electrical connections between fin-type transistors.

Aller teaches individual source/drain regions (32) in the plurality of the semiconductor layers are electrically commonly connected (25) and the gate electrode(s) (90) is formed such that the gate electrode(s) strides over the commonly connected semiconductor layers (Fig. 2B Col. 4 lines: 10-23); and the first semiconductor region further comprises a connecting semiconductor layer which protrudes upward from the substrate and electrically commonly connects source/drain regions of at least two of the plurality of the semiconductor layers by extending in the direction perpendicular to the channel current direction; and the gate electrode(s) is formed such that the gate electrode(s) strides over the semiconductor layers connected by the connecting semiconductor layer (Fig. 2B Col. 4 lines: 10-23).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device as disclosed by Achuthan by incorporating gate electrode arrangement and source/drain connections as taught by Aller. The motivation would have been to increase channel area by using multiple fins (Aller – Col. 4 lines: 10-23).

7. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over US Achuthan, in view of US 2005/0145932 (hereinafter "Park")

Regarding claim 12, Achuthan teaches a device comprising a first and second semiconductor region, but does not mention the gate contact is formed over the second region.

Park teaches a contact (124b Fig. 33) with the gate electrode(s) (124a Fig. 33) is formed over the semiconductor layers in the second semiconductor region (para [0057]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device as disclosed by Achuthan by incorporating gate electrode contact as taught by Park. The motivation would have been to avoid short channel effects caused by the gate electrode (Park - para [004]).

8. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over US Achuthan, in view of US 2005/0145932 (hereinafter "Park")

Regarding claim 24, Achuthan teaches forming a device comprising a first and second semiconductor region, but does not mention forming the gate contact is over the second region.

Park teaches that in the step of forming the transistor, a contact (124b Fig. 33) with the gate electrode(s) (124a Fig. 33) is further formed over the semiconductor layers in the second semiconductor region to which the gate electrode(s) extends (para [0057]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by Achuthan by incorporating gate

electrode contact forming step as taught by Park. The motivation would have been to avoid short channel effects caused by the gate electrode (Park - para [004]).

9. **Claim 26**, is rejected under 35 U.S.C. 103(a) as being unpatentable over US Achuthan, in view of Fried.

Regarding claim 26, Achuthan teaches a separate source/drain regions and a separate gate electrode formed on a semiconductor layer in the first semiconductor region, but does not explicitly teach a plurality of semiconductor layers with separate source/drain regions and separate gate electrodes.

10. Fried teaches that in the step of forming the transistor, a plurality of the gate electrodes (222) are formed such that each gate electrode strides over one semiconductor layer in the first semiconductor region (Fig. 7, Col. 8 lines: 60-66, Col. 9 lines: 1-2).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the process as disclosed by Achuthan by incorporating a plurality of gate electrodes as taught by Fried. The motivation would have been to use FinFETs based logic devices (Fried – Col. 9 lines: 3-39).

11. **Claim 28**, are rejected under 35 U.S.C. 103(a) as being unpatentable over US Achuthan, in view of Aller.

Regarding claim 28, Achuthan teaches forming a source/drain regions and a gate electrode on a semiconductor layer in the first semiconductor region, but does not

explicitly teach forming arrangements of gate electrode(s) and electrical connections between fin-type transistors.

Aller teaches the process wherein in the step of forming the fin-type semiconductor layers, a connecting semiconductor layer is further formed as the first semiconductor region, which protrudes upward from the substrate, extends in a direction perpendicular to the channel current direction and electrically commonly connects at least two of the plurality of the semiconductor layers; and wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) strides over the semiconductor layers connected by the connecting semiconductor layer (Fig. 2B Col. 4 lines: 10-23).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by Achuthan by incorporating gate electrode and source/drain connection forming step as taught by Aller. The motivation would have been to increase channel area by using multiple fins (Aller – Col. 4 lines: 10-23).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andres Munoz whose telephone number is (571) 270-3346. The examiner can normally be reached on 7:30am - 4:00pm (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anh Mai can be reached on (571) 272-1995. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh T. Mai/
Supervisory Patent Examiner,
Art Unit 4148

/Andres Munoz/
Examiner, Art Unit 4148
April 8, 2009